



MS-7693

Ver:2.0

CPU

AMD M3 Phenom/Athlon 64 FX AM3/AM3R2

System Chipset

AMD RX980

ATI SB950

On Board Chip

FINTEK Super I/O -- F71889AD

LAN -- RTL8111EL

HD Codec --ALC892

ASM1042 USB3.0

BIOS -- SPI ROM 32M

Main Memory

DDR III X 4 (Max 32GB)

Expansion Slots

PCI-E X 16*1

PCI-E X 8 *1

PCI-E X 1 *2

PCI 2.2 Slot X 2

PWM

Controller--IUPI1601 4+1 Phase

Vcore 4 Phase (MOS HIGHX2 LOWX2)

Vnb 1 Phase (MOS HIGHX1 LOWX2)

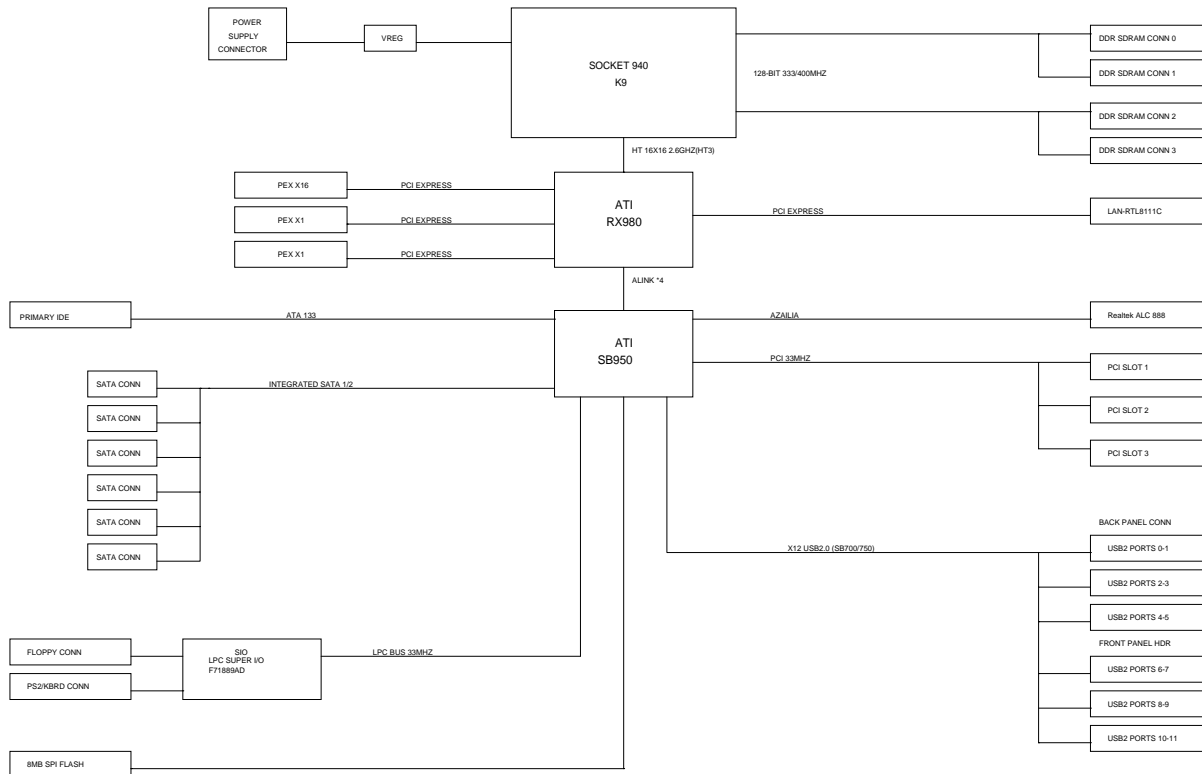
Clock Generator

Controller--RTM880N-793

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Micro Star Restricted Secret		
Title	Cover Sheet	Rev
Document Number	MS-7693	2.0
MICRO-STAR INT'L CO., LTD. No. 69, Li-Chi St., Jung-Hsi City, Taichung Hsien, Taiwan http://www.msi.com.tw		Last Revision Date: Tuesday, September 13, 2011
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BLOCK DIAGRAM

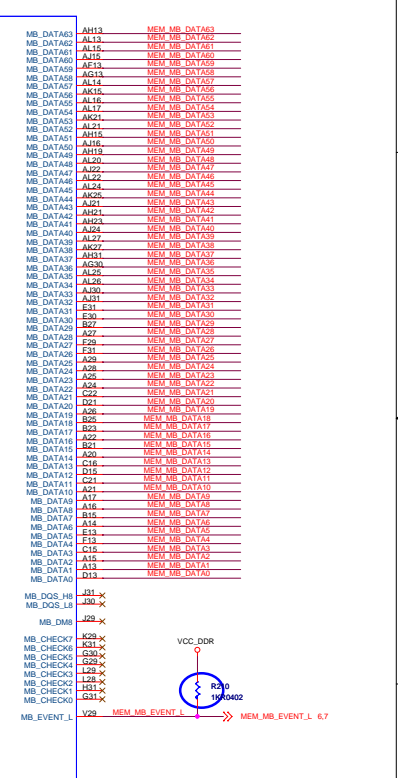
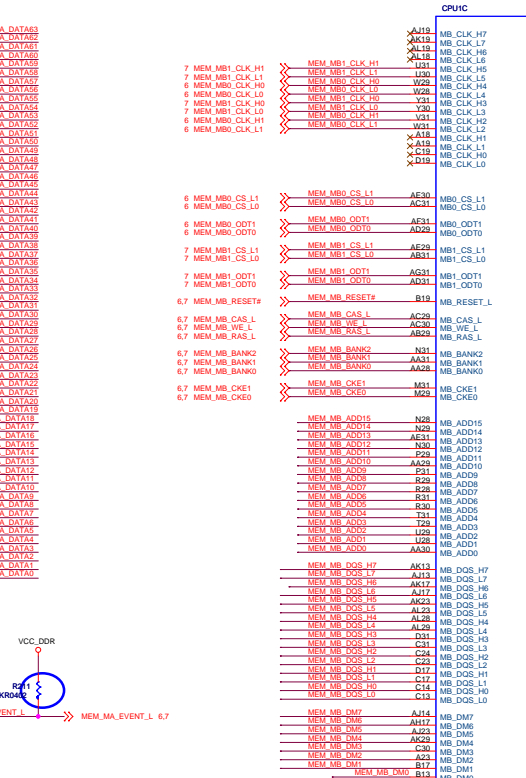
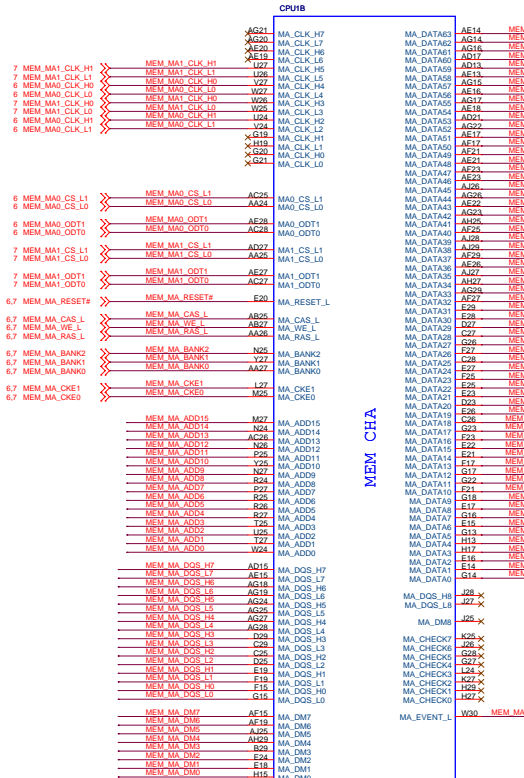


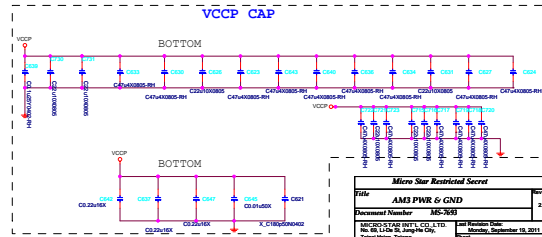
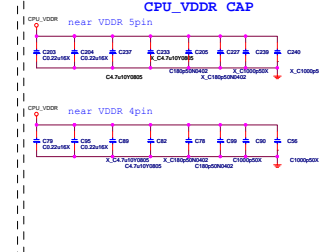
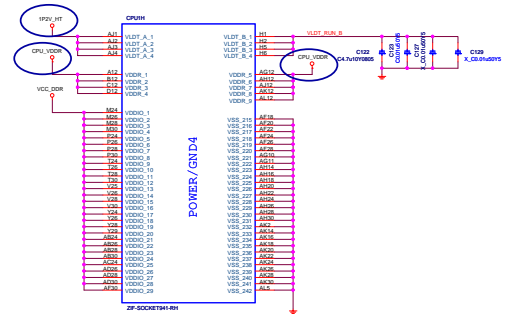
www.schematic-x.blogspot.com

Micro Star Restricted Secret			
Title		Rev	
Block Diagram		2.0	
Document Number		MS-7693	
MICRO-STAR INT'L CO., LTD. No. 49, Li-Chi St., Jung-Hsi City, Taipei Hsien, Taiwan http://www.msi.com.tw		Last Revision Date: Tuesday, September 13, 2011	
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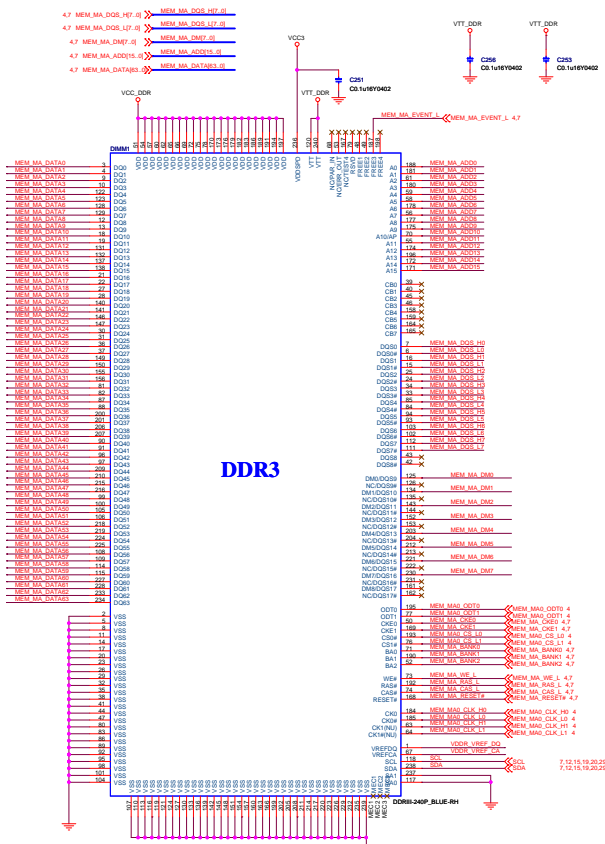
6.7 MEM_MA_DQS_L[7..0] MEM_MA_DQS_L[7..0]
 6.7 MEM_MA_DQS_H[7..0] MEM_MA_DQS_H[7..0]
 6.7 MEM_MA_DM[7..0] MEM_MA_DM[7..0]
 6.7 MEM_MA_ADD[15..0] MEM_MA_ADD[15..0]
 6.7 MEM_MA_DATA[63..0] MEM_MA_DATA[63..0]

6.7 MEM_MB_DQS_L[7..0] MEM_MB_DQS_L[7..0]
 6.7 MEM_MB_DQS_H[7..0] MEM_MB_DQS_H[7..0]
 6.7 MEM_MB_DM[7..0] MEM_MB_DM[7..0]
 6.7 MEM_MB_ADD[15..0] MEM_MB_ADD[15..0]
 6.7 MEM_MB_DATA[63..0] MEM_MB_DATA[63..0]





Micro Star Restricted Secret	
Title	AM3 PWR & GND
Document Number	MS-763
MICRO-STAR INT'L CO., LTD. No. 69, Li-Chai St., Jung-Hsi City, Taichung Hsien, Taiwan http://www.msi.com.tw	and Revision Date: Monday, September 10, 2011 Sheet 5 of 37

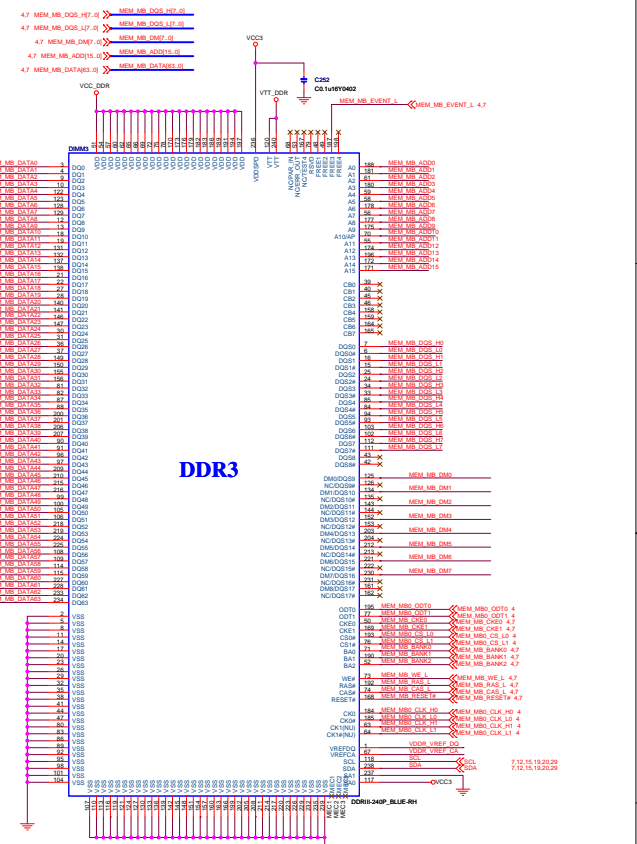


DDR3

ADDRESS A0

SMBus Addressing

Device	8-bit Address (hex)
D198A0	A0
D198B0	A2
D198A1	A4
D198B1	A6



DDR3

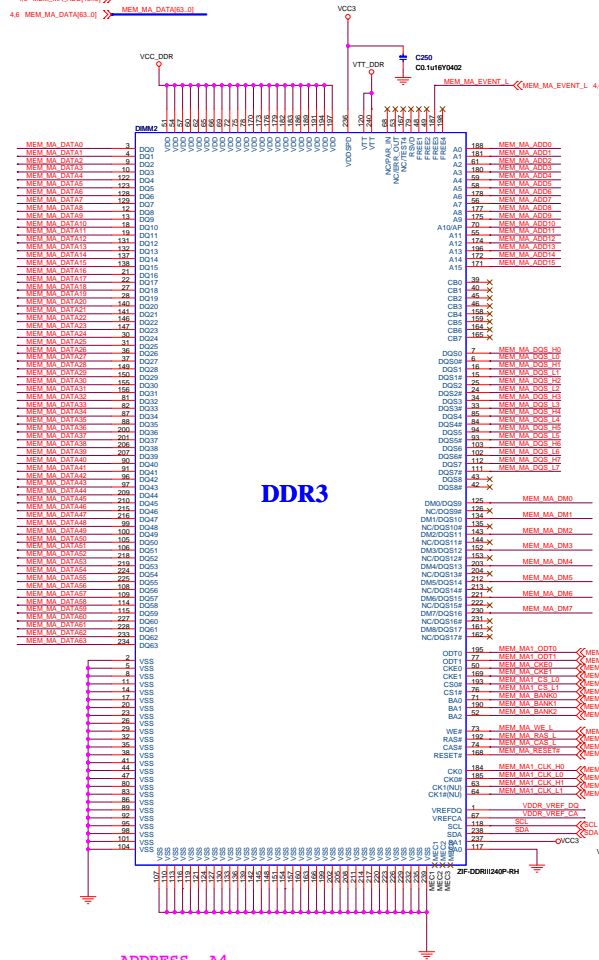
ADDRESS A2

SMBus Addressing

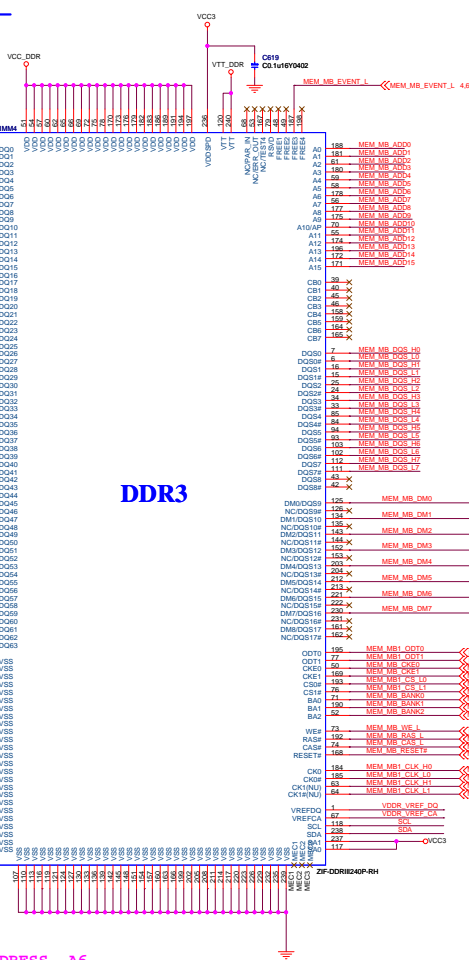
Device	8-bit Address (hex)
D198A0	A0
D198B0	A2
D198A1	A4
D198B1	A6

MEM_MA_DQS_H47.GI
MEM_MA_DQS_L47.GI
MEM_MA_DM7.GI
MEM_MA_ADD15.GI
MEM_MA_DATA03.GI

MEM_MB_DQS_L17.GI
MEM_MB_DQS_H47.GI
MEM_MB_DM7.GI
MEM_MB_ADD15.GI
MEM_MB_DATA03.GI

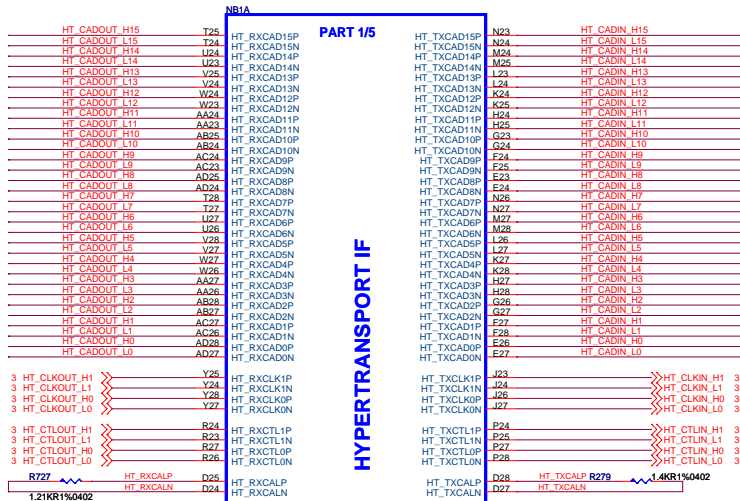


ADDRESS A4



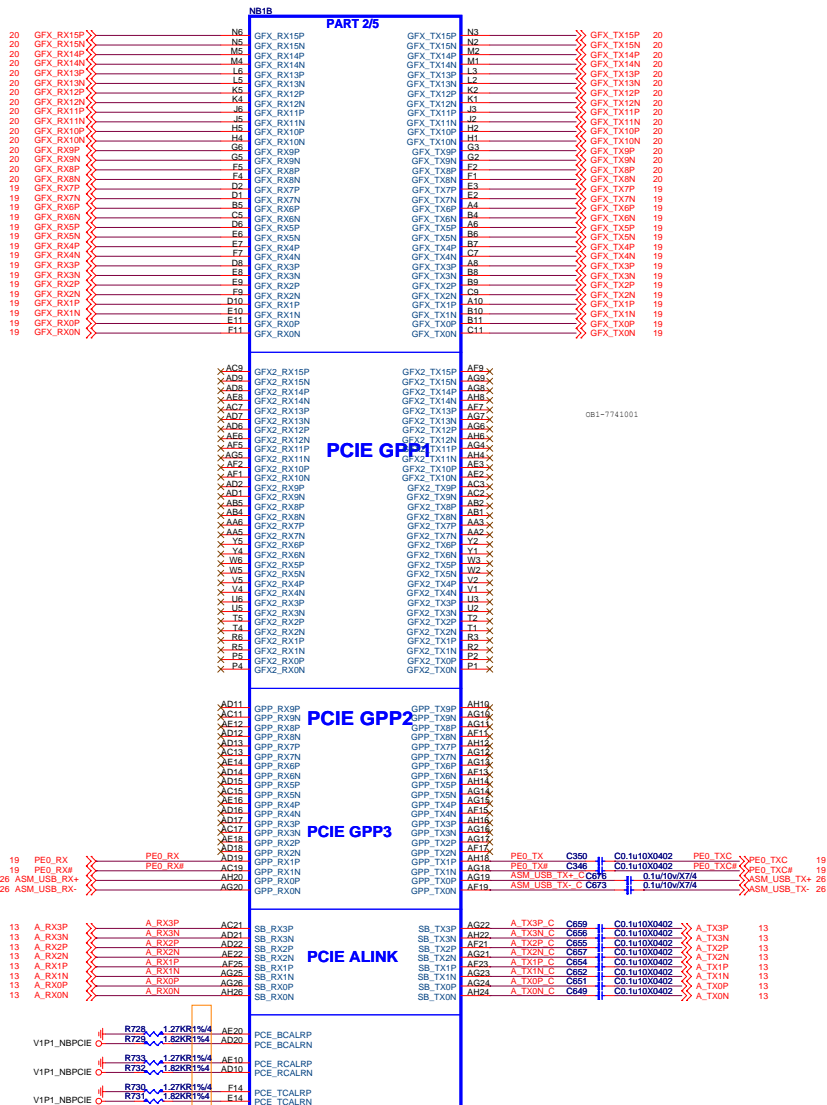
ADDRESS A6

3 HT_CADIN_H[15..0] >> HT_CADIN_H[15..0]
3 HT_CADIN_L[15..0] >> HT_CADIN_L[15..0]
3 HT_CADOUT_H[15..0] >> HT_CADOUT_H[15..0]
3 HT_CADOUT_L[15..0] >> HT_CADOUT_L[15..0]

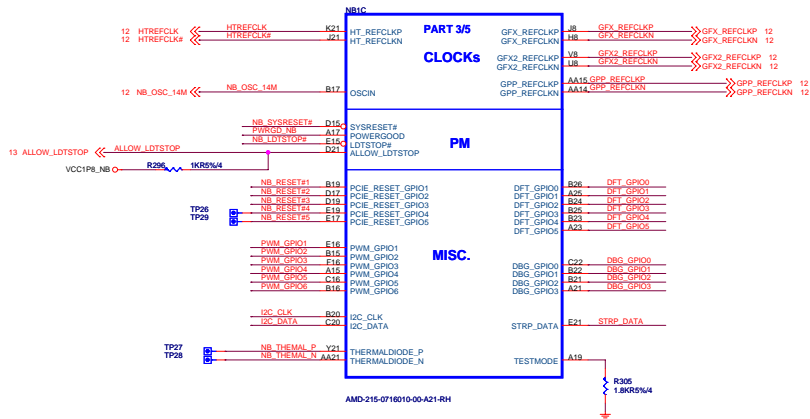


AMS-215-0716010-00-A21-RH

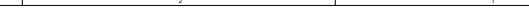
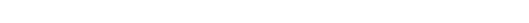
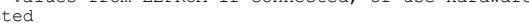
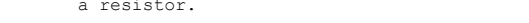
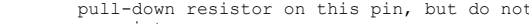
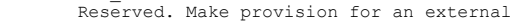
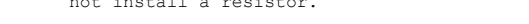
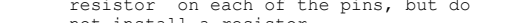
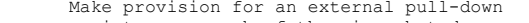
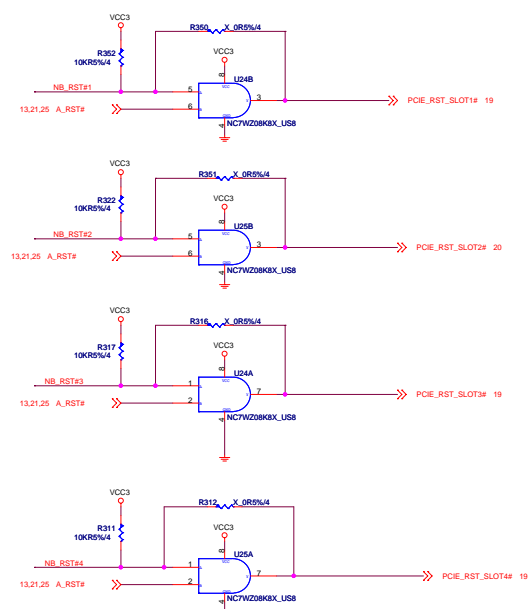
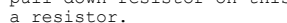
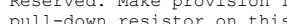
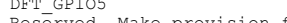
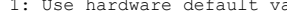
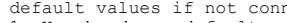
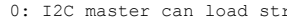
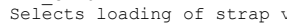
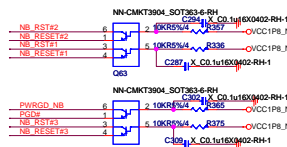
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Title	RD780-HT LINK I/F	Rev 2.0
Document Number	MS-7963	
MICRO-STAR INT'L CO.,LTD. No. 69, Li-De St, Jung-Ho City, Taipei Hsien, Taiwan http://www.msi.com.tw		Last Revision Date: Wednesday, September 14, 2005 Sheet 8 of 37



Spacing : 6mil



DFT_GPIO[4:2]	STRAP_PCIE_GPP_CFG	Mode
1111	1-1-1-1-1-1	Mode L
1101	1-1-1-1-1-0	Mode L
1011	2-0-0-0-0-2-0	Mode C2
1001	2-0-0-0-0-1-0	Mode L
0111	2-0-1-1-1-1-1	Mode L
0110	1-1-1-1-1-1-1	Mode L
0011	4-0-0-0-0-1-1	Mode C
0001	4-0-0-0-0-2-0	Mode B

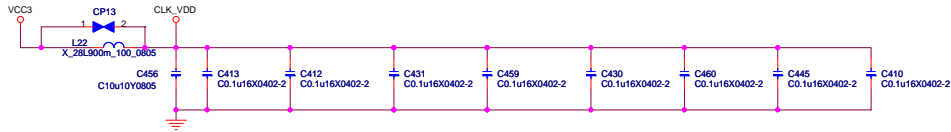


PWM_GPIO[5:2]
Reserved.
Make provision for an external pull-down resistor on each of the pins, but do not install a resistor.

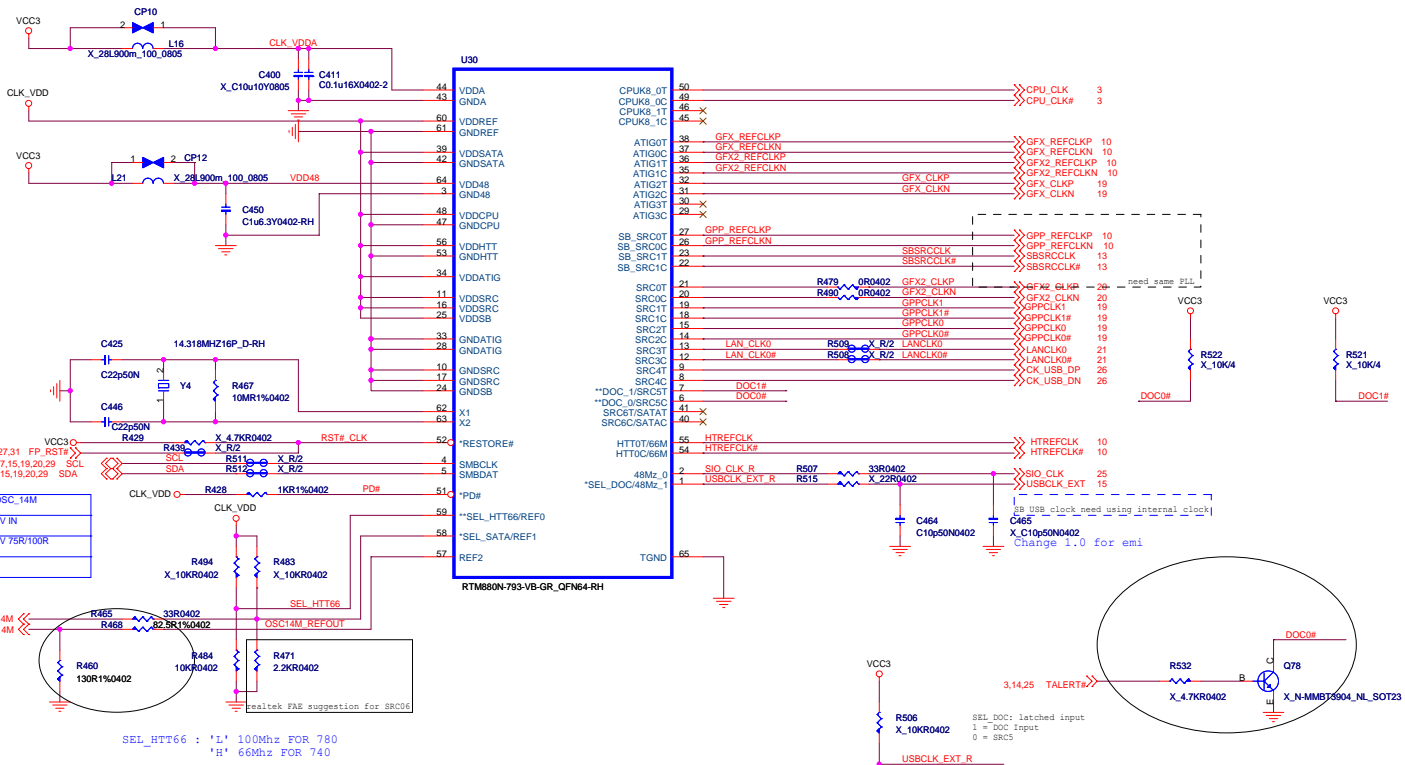
DFT_GPIO0
Reserved. Make provision for an external pull-down resistor on this pin, but do not install a resistor.

DFT_GPIO5
Reserved. Make provision for an external pull-down resistor on this pin, but do not install a resistor.

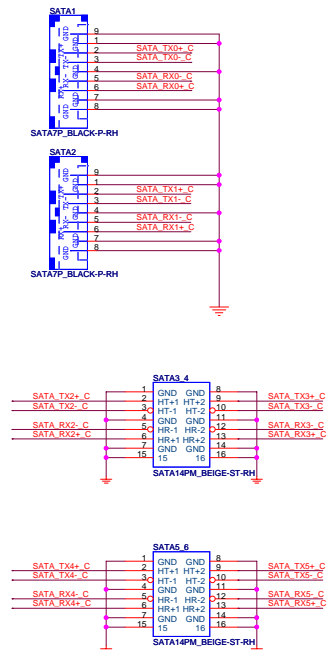
Micro Star Restricted Secret		
Title	RD780-SYSTEM I/F	Rev
Document Number	MS-7693	2.0
MICRO-STAR INT'L CO., LTD.		
No. 60, LiDe St., Jung-Hsue City,		
Tapei Hsien, Taiwan		
http://www.msi.com.tw		
Last Revision Date:		Thursday, October 20, 2011
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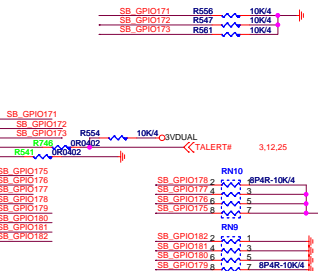
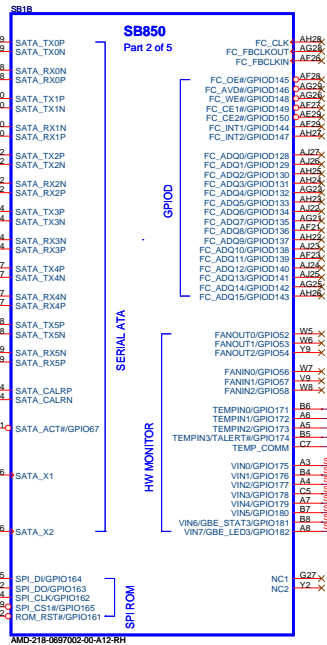
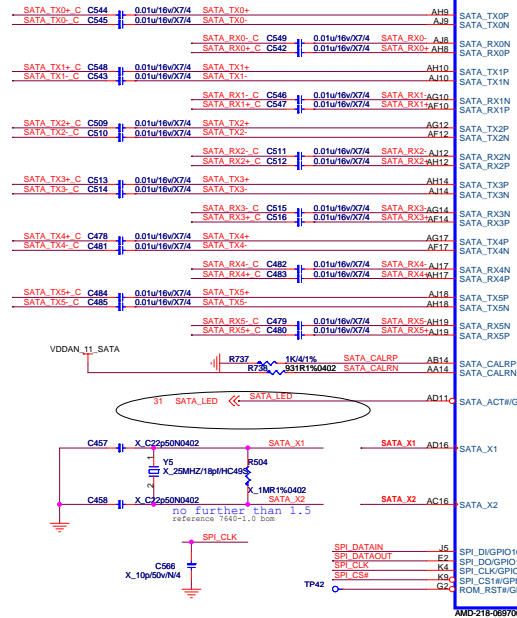
- 1- PLACE ALL THE SERIES TERMINATION RESISTORS AS CLOSE AS U19 AS POSSIBLE
- 2- ROUTE ALL CPUCLK/#, NBSRCLK/#, GPPCLK/# AS DIFFERENT PAIR RULE
- 3- PUT DECOUPLING CAPS CLOSE TO U19 POWER PIN



Micro Star Restricted Secret		
Title	Clock Generator RTM880N-793	Rev 2.0
Document Number	MS-7693	
MICRO-STAR INT'L CO. LTD. No. 68, Li-De St, Jung-He City, Taipei Hsien, Taiwan		Last Revision Date: Wednesday, September 14, 2011
http://www.msi.com.tw		Sheet 12 of 37



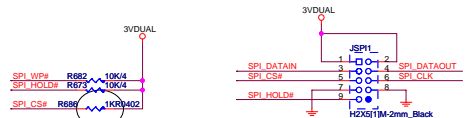
SATA_TX[5:0]P/N: Routed with 90-ohm \pm 10% differential impedance.
 SATA_RX[5:0]P/N: Routed with 90-ohm \pm 10% differential impedance.
 Gen3: Signal length from the Southbridge to connector \leq 2.5".



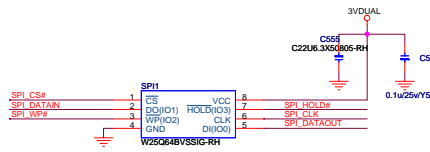
SPI FLASH MEMORY

SPI DEBUG PORT

Place close to SPI ROM



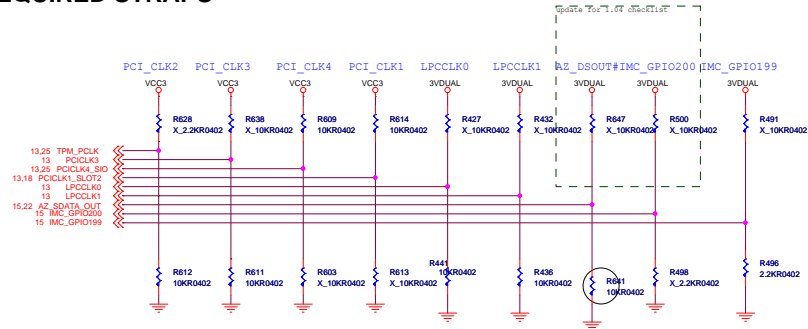
Part Number : N31-2051451-H06



Micro Star Restricted Secret	
Title	SB700-SATA/IDE/HWM/SPI
Document Number	MS-7693
MICRO-STAR INT'L CO. LTD.	Last Revision Date: Wednesday, October 19, 2011
No. 65, Li-De St., Jung-Ho City, Taipei, Taiwan	Sheet
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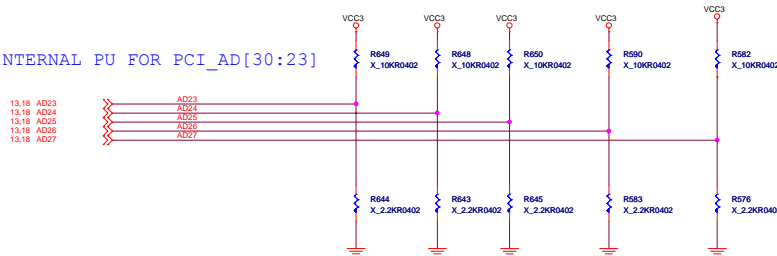
REQUIRED STRAPS

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC_CLK



	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	AZ_DSOUT#IMC_GPIO200	IMC_GPIO199
PULL HIGH	ALLOW PCIE GEN2 DEFAULT	WATCHDOG TIMER ON NB_PWRGD ENABLED DEFAULT	USE DEBUG STRAPS DEFAULT	NON-FUSION CPU CLOCK MODE DEFAULT	UEC ENABLE DEFAULT	CLKGEN ENABLED DEFAULT	PERFORMANCE MODE DEFAULT	ROM TYPE: H, H = Reserved H, L = SPI ROM L, H = LPC ROM L, L = FWH ROM
PULL LOW	FORCE PCIE GEN1	WATCHDOG TIMER ON NB_PWRGD DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT	FUSION CPU CLOCK MODE DEFAULT	DISABLE EC DEFAULT	CLKGEN DISABLED DEFAULT	PERFORMANCE MODE DEFAULT	

SB800 HAS 15K INTERNAL PU FOR PCI_AD[30:23]



DEBUG STRAPS

	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

Micro Star Restricted Secret		
Title	SB950-STRAPS	Rev 2.0
Document Number	MS-7693	
MICRO-STAR INT'L CO. LTD. No. 69, Li-De St., Jung-Ho City, Taipei Hsien, Taiwan http://www.msi.com.tw		Last Revision Date: Wednesday, September 14, 2011 Sheet 17 of 37

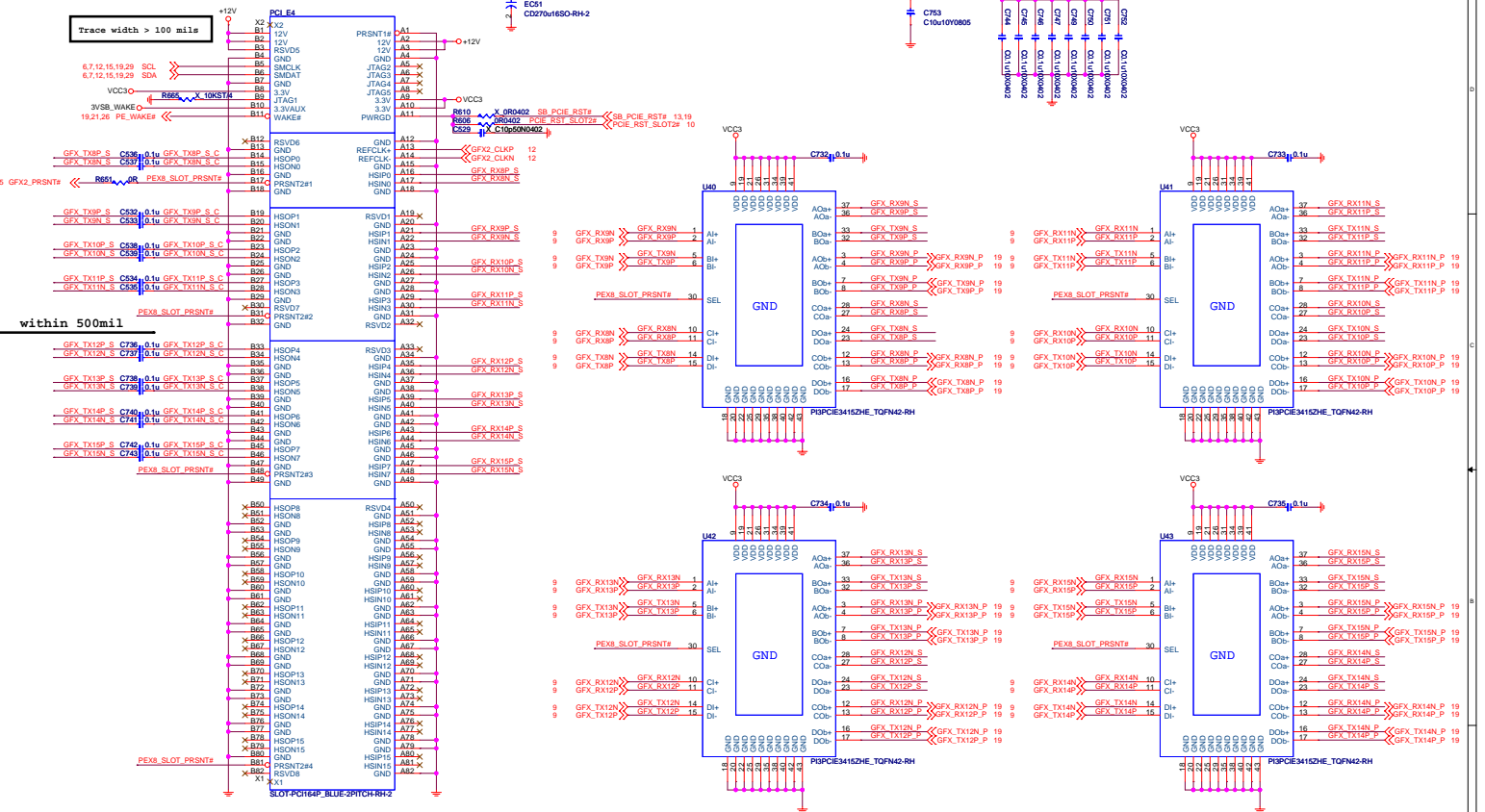
PCI F2



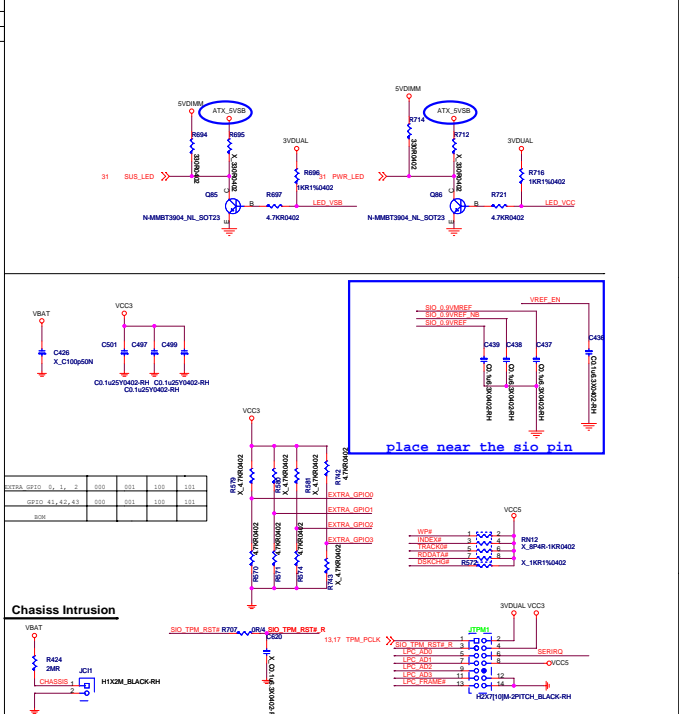
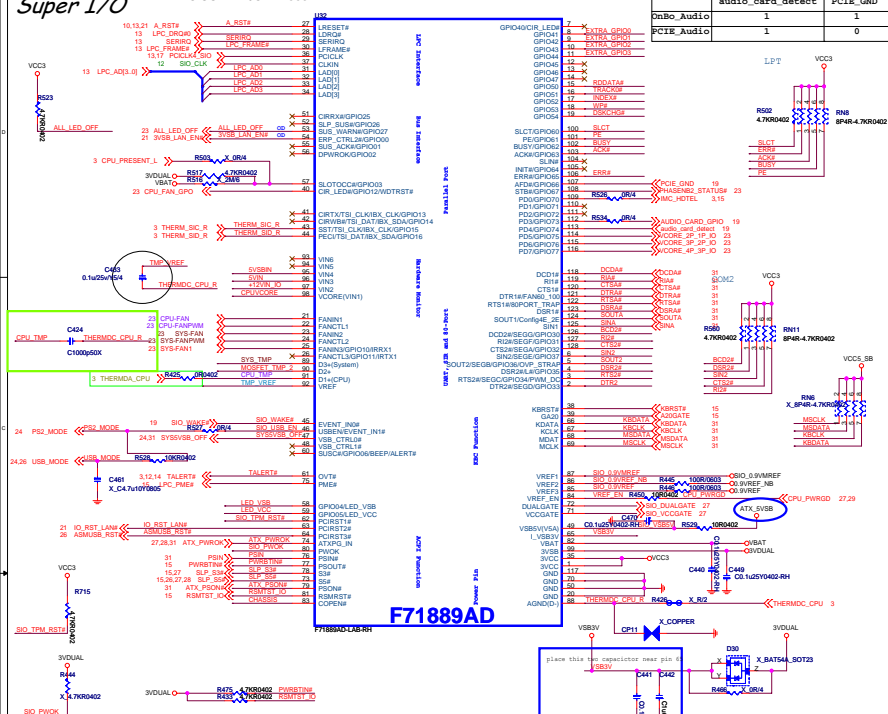
Title <i>PCI-E X16 , X1 Slot</i>		Rev 2.0
Document Number MS-7693		
MICRO-STAR INT'L CO.,LTD. No. 69, Li-De St, Jung-Ho City, Taipei Hsien, Taiwan http://www.msi.com.tw		Last Revision Date: Tuesday, October 18, 2011 Sheet <div style="display: flex; justify-content: space-around;"> 19 of 37 </div>

PCI EXPRESS X8 SLOT

near PCIe X8



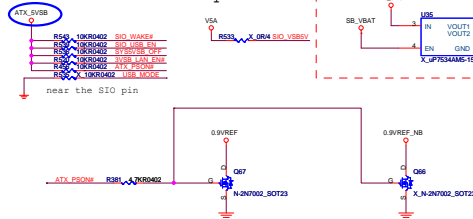
Micro Star Restricted Secret		
Title	PCIE X1 Slot 1_2	Rev 2.0
Document Number	MS-7693	
MICRO-STAR INT'L CO., LTD.		
No. 69, Li-Chi St., JungHe City,		
Taipei Hsien, Taiwan		
http://www.msi.com.tw		
Last Revision Date:	Tuesday, October 26, 2011	
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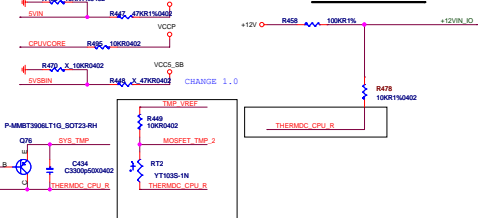
LPC I/O STRAPPING RESISTOR



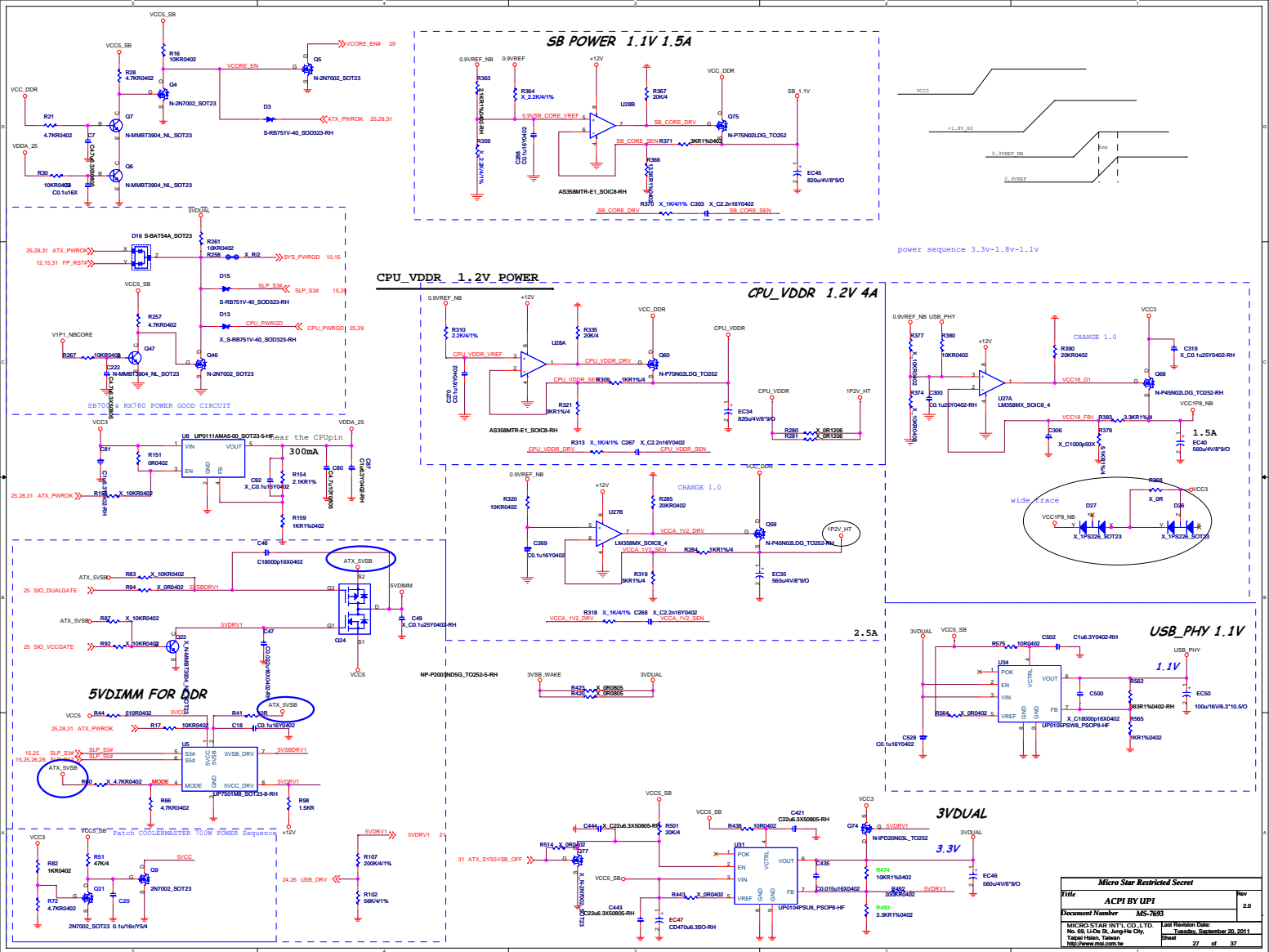
	Don't STUFF	STUFF
RTS2#	90M FAN	LINEAR FAN
RTSA#	80Port enable	80Port disable
SOUTA	4E	2E
DTRA#	FAN START DUTY 60%	FAN START DUTY 100%
SOUT2	Disable alarm mode	Enable force mode



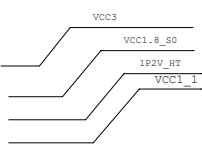
Thermal Resistor



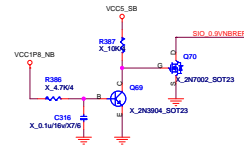
NOTE: LOCATE CLOSE S VRM mosfet ,for VRM mosfet temperature detect only



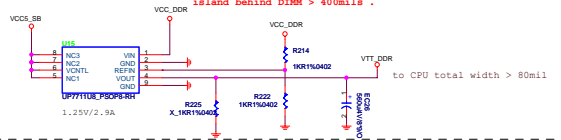
RX780 power up sequence



Reserve for RX980 POS



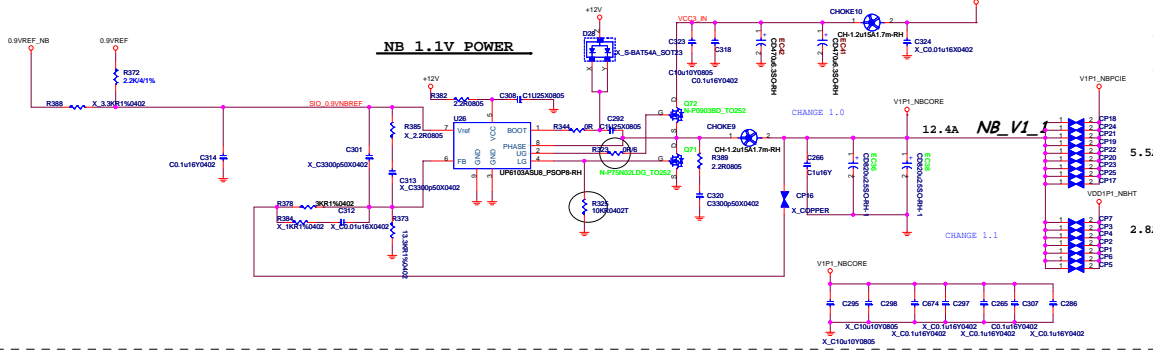
DDR VTT Power



To CPU Copper trace width > 250mils, Fill island behind DIMM > 400mils.

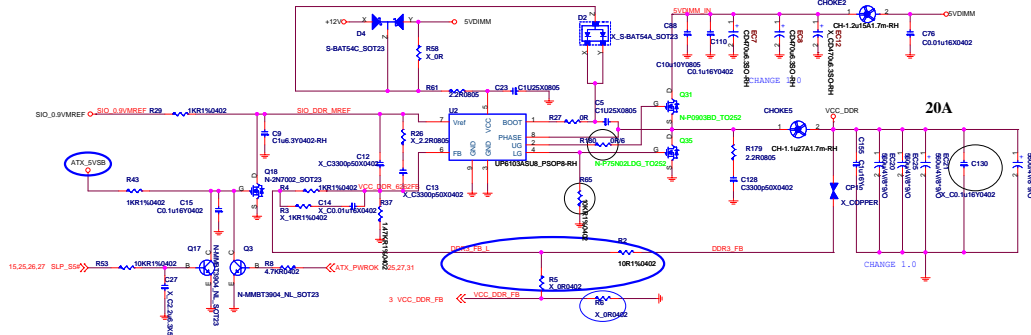
to CPU total width > 80mmil

NB 1.1V POWER



H-MOS: D03-0903BDB-N03
AVL: D03-0480900-005
L-MOS: D03-75N022B-N03
AVL: D03-0480600-005

DDR III 1.5V POWER



VCC_DDR

20A

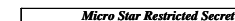
Micro Star Restricted Secret		
Title	VCC_DDR&VCC1_1	Rev 2.0
Document Number	MS-7693	
MICROSTAR INT'L CO. LTD. No. 99, Udaan Rd., Song-Shan City, Taippei Hsien, Taiwan		
First Revision Date: September 20, 2011		Page 20 of 37

Intel Front Panel

ESD Protect

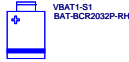
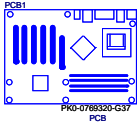
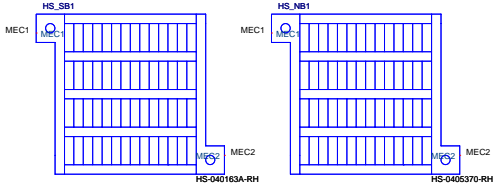


Trace Width 80mils.

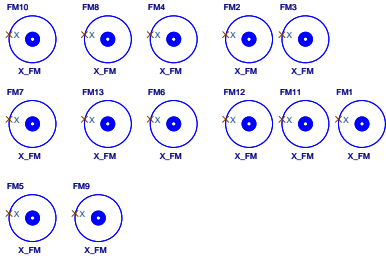


Title	Rev
ATX connector / Front Panel/KB	2.0
Document Number	
MS-7693	
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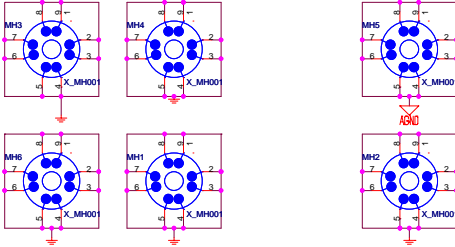
MK1
G81-MHS-P93-Q13



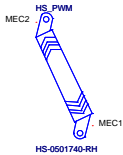
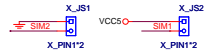
Optics Orientation Holes



Mounting Holes



Simulation



Micro Star Restricted Secret		
Title	MANUAL PARTS	Rev 2.0
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